L Number	Hits	Search Text	DB	Time stamp
1	959869	TAP interface with STP interface	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:33
2	821654	TAP/STP interface$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:33
3	812532	(TAP interface with STP interface) and (TAP/STP interface$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:33
4	925	"IEEE 1149.1"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:33
5	748	((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:34
6	3789571	integrated circuit	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:34
7	721	(((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:37
8	4699725	single mode test access port$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:37
9	3557090	dual mode test access port$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:37
10	721	((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:47
11	3673415	TAP clock circuit	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:48
12	3009849	data register$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:49

13	715	(((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:49
14	881110	instruction register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:49
15	694	((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:49
16	664	(((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:50
17	130773	multiplexer$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:50
18	407	((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:51
19	1257443	TAP controller	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:51
20	358	(((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:51
21	2219415	scan test port	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:52
22	357	((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:55
23	1704259	scan path	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:55
24	354	((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:55

25	871331	core$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:55
26	203	((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:56
27	822348	scan register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:57
28	203	((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:58
29	139253	accessing and (data register with first access protocol)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:59
30	125	((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)) and (accessing and (data register with first access protocol))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:59
31	139247	accessing and (data register with second access protocol)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:59
32	125	((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)) and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:00
33	1560115	test instruction	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01
34	125	((((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)) and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and (test instruction)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01

35	544856	in-circuit emulation register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01
36	544857	((((((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)) and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and (test instruction)) afnd (in-circuit emulation register)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01
37	669813	in-circuit programming register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01
38	537545	((((((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)) and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and (test instruction)) afnd (in-circuit emulation register)) and (in-circuit programming register)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:02
39	1123557	boundary scan register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:02
40	683998	bypass register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:03
41	545759	(boundary scan register) and (bypass register)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:03
42	534086	((((((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)) and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and (test instruction)) afnd (in-circuit emulation register)) and (in-circuit programming register)) and ((boundary scan register) and (bypass register))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:05
43	5468563	select$4 dual mode test access port	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:05

44	338696	((((((((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)) and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and (test instruction)) afnd (in-circuit emulation register)) and (in-circuit programming register)) and ((boundary scan register) and (bypass register))) and (select$4 dual mode test access port)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:06
45	5009	714/724.ccls. or 714/725.ccls. or 714/727.ccls. or 714/733.ccls. or 714/734.ccls. or 714/30.ccls. or 714/726.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:08
46	2324	((((((((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)) and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and (test instruction)) afnd (in-circuit emulation register)) and (in-circuit programming register)) and ((boundary scan register) and (bypass register))) and (select$4 dual mode test access port)) and (714/724.ccls. or 714/725.ccls. or 714/727.ccls. or 714/733.ccls. or 714/734.ccls. or 714/30.ccls. or 714/726.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:09
47	107	714/729.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:09
48	60	((((((((((((((((((TAP interface with STP interface) and (TAP/STP interface$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port$1) with (dual mode test access port$1))) and (data register$1)) and (instruction register)) and (TAP clock circuit)) and multiplexer$1) and (TAP controller)) and (scan test port)) and (scan path)) and core$1) and (scan register)) and (accessing and (data register with first access protocol))) and (accessing and (data register with second access protocol))) and (test instruction)) afnd (in-circuit emulation register)) and (in-circuit programming register)) and ((boundary scan register) and (bypass register))) and (select$4 dual mode test access port)) and (714/724.ccls. or 714/725.ccls. or 714/727.ccls. or 714/733.ccls. or 714/734.ccls. or 714/30.ccls. or 714/726.ccls.)) and 714/729.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:09